## AMENDMENT TRANSMITTAL LETTER

Docket No. M4065.0014/P014 B

Application No.	Filing Date	Examiner	Art Unit
09/940,791	August 29, 2001	Kiesha L. Rose	2822

Applicant(s): Larry D. Kinsman

Invention: LOW PROFILE BALL GRID ARRAY PACKAGE

## TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

		CLAIM	S AS AMEND	ED	
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	7	- 20 =		x	0.00
Independent Claims	3	- 3 =		х	0.00
Multiple Depen	dent Claims (ch	eck if applicab	le)		
Other fee (pleas	se specify):				
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00
x Large Entity	/			Small Entity	
X No addition	al fee is require	d for this ame	ndment.		
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Please charge Deposit Account No A duplicate copy of this sheet is enclosed.	in the amount of \$
A check in the amount of \$	to cover the filing fee is enclosed.
Payment by credit card. Form PTO-2038 is	attached.
The Commissioner is hereby authorized to as described below. A duplicate copy of the	
x Credit any overpayment.	
x Charge any additional filing or application	processing fees required under 37 CFR 1.16 and 1.17.
msde	Dated: December 11, 2002
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Docket No.: M4065.0014/P014-B (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Larry D. Kinsman

Application No.: 09/940,791

Filed: August 29, 2001

For: LOW PROFILE BALL GRID ARRAY

**PACKAGE** 

Group Art Unit: 2822

Examiner: Kiesha L. Rose

## AMENDMENT UNDER 37 CFR § 1.116

ATTN: Box AF

Commissioner for Patents Washington, DC 20231

Dear Sir:

Responsive to the Office Action of September 11, 2002, finally rejecting claims 39-44, please amend the above-identified U.S. patent application as follows:

## IN THE CLAIMS:

Please replace claims 39-44 with amended claims 39-44.

39. (twice amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface,